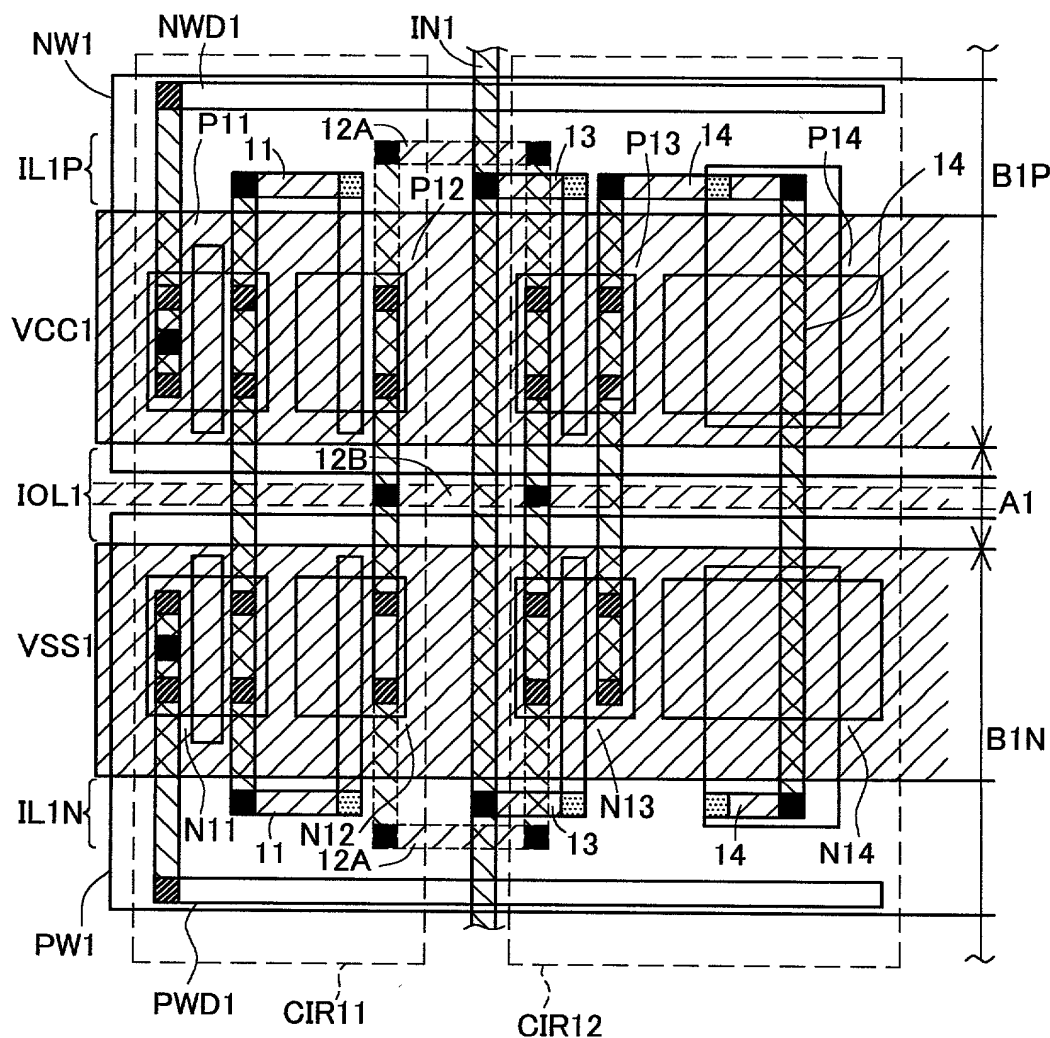


FIG.1

LAYOUT DIAGRAM DIRECTED TO FIRST EMBODIMENT



- CONTENTS OF CONTACT
- BETWEEN FIRST METAL LAYER AND SECOND METAL LAYER (C_v)
 - ▤ BETWEEN SECOND METAL LAYER AND POLY-SILICON (C_{pp})
 - ▨ BETWEEN FIRST METAL LAYER AND DEFFUSED LAYER

FIG.2

LAYOUT DIAGRAM DIRECTED TO SECOND EMBODIMENT

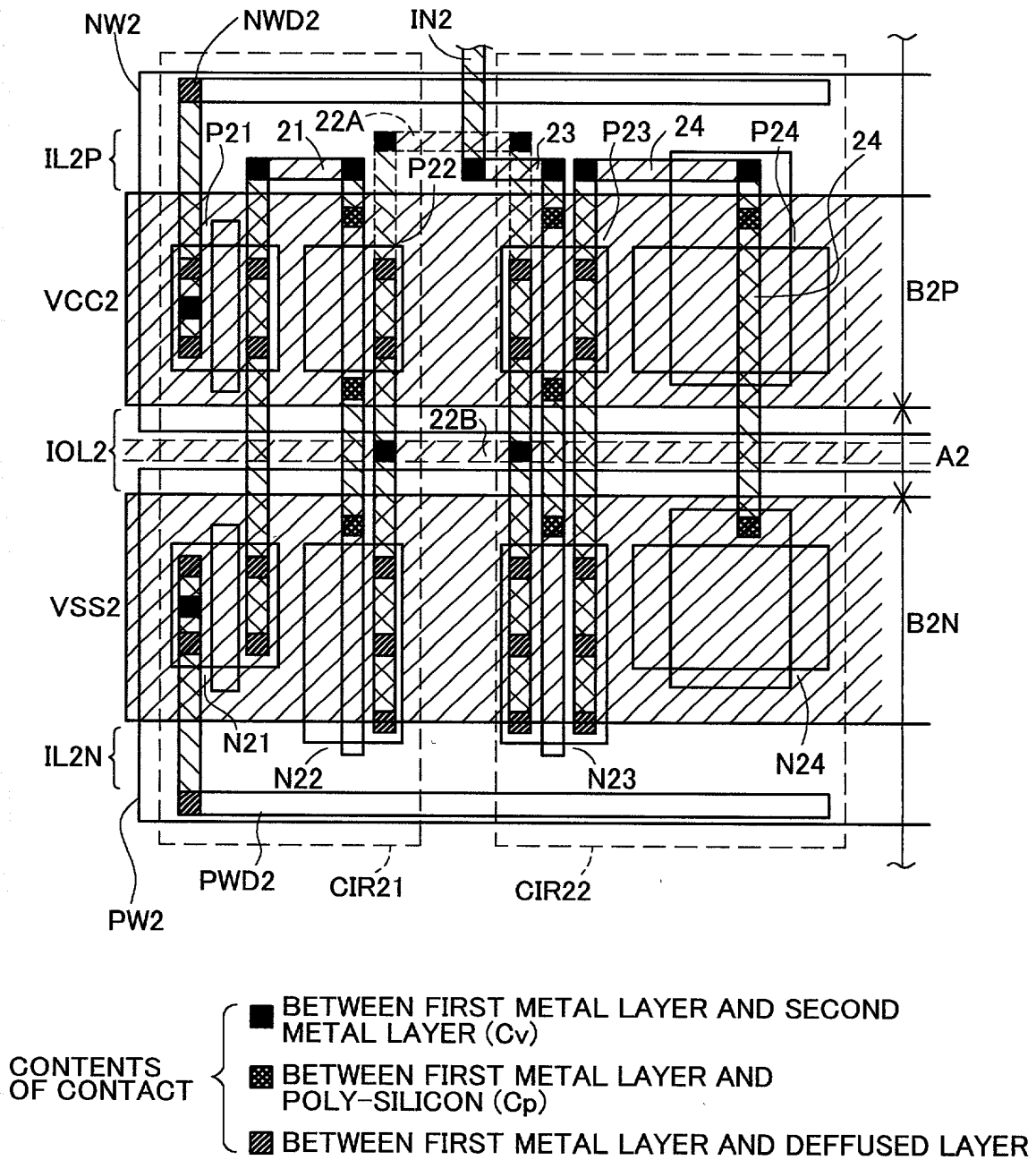


FIG.3

LAYOUT DIAGRAM DIRECTED TO THIRD EMBODIMENT

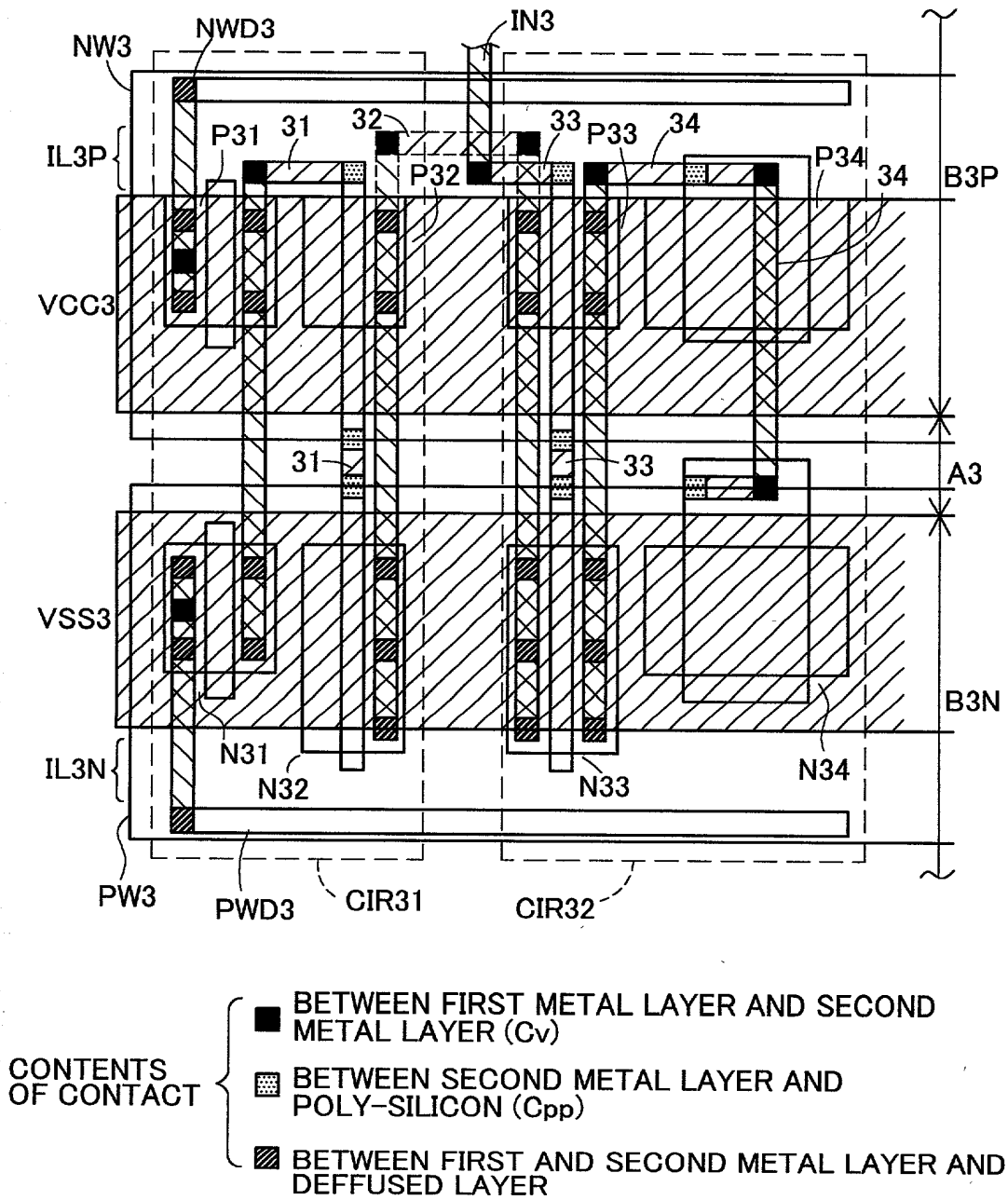
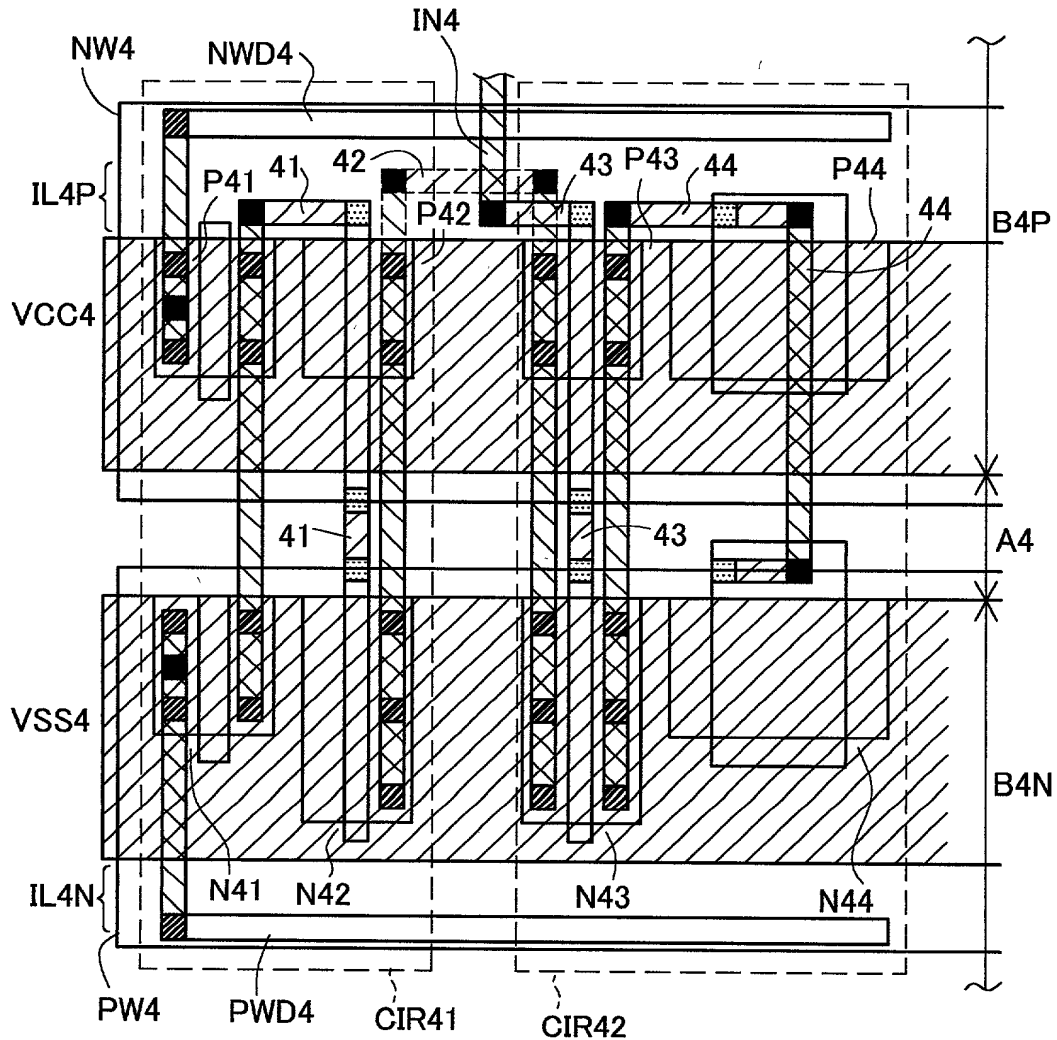


FIG.4

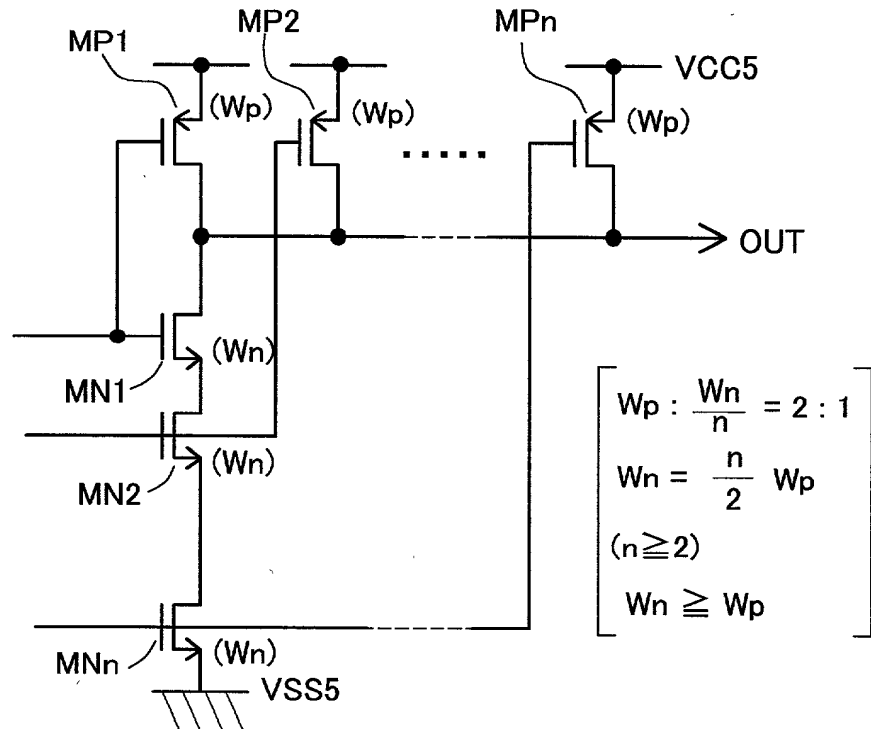
LAYOUT DIAGRAM DIRECTED TO FOURTH EMBODIMENT



- CONTENTS OF CONTACT
- BETWEEN FIRST METAL LAYER AND SECOND METAL LAYER (C_v)
 - ▤ BETWEEN SECOND METAL LAYER AND POLY-SILICON (C_{pp})
 - ▨ BETWEEN FIRST METAL LAYER AND DEFFUSED LAYER

FIG.5

RELATIONSHIP BETWEEN UNIT WIRING REGION AND
LAYOUT OF NAND GATE (FIFTH EMBODIMENT)



↓ $(n = 4 : W_n = 2W_p)$

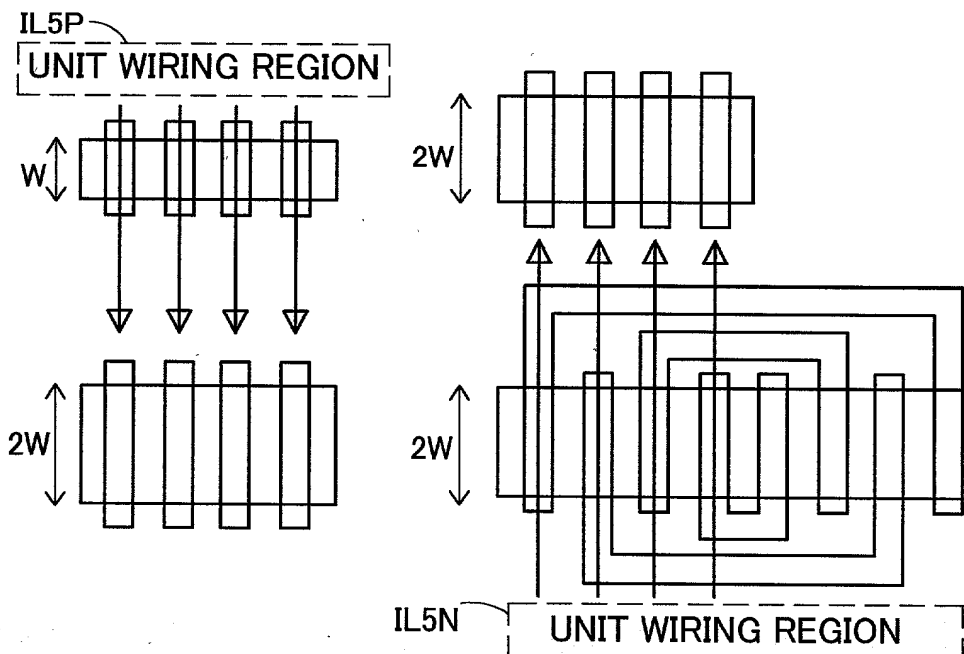
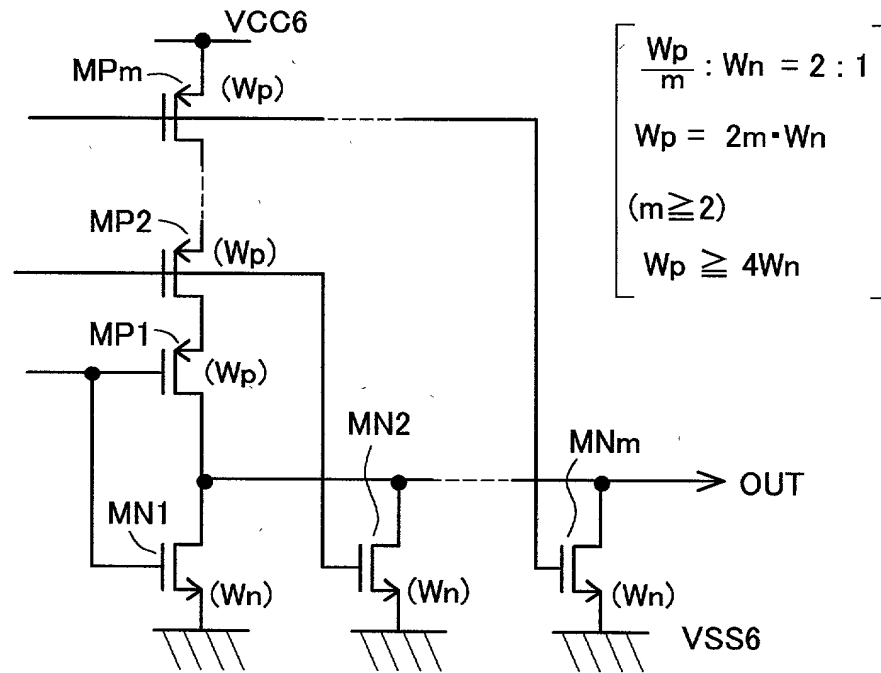


FIG.6

RELATIONSHIP BETWEEN UNIT WIRING REGION AND
LAYOUT OF NOR GATE (SIXTH EMBODIMENT)



↓ (n = 2 : $W_p = 4W_n$)

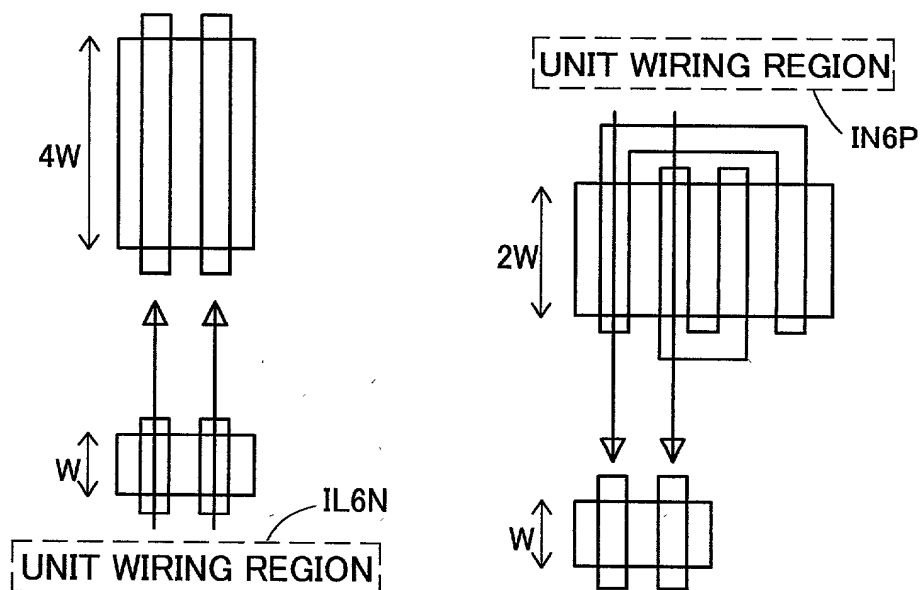


FIG.7

LAYOUT DIAGRAM DIRECTED TO SEVENTH EMBODIMENT

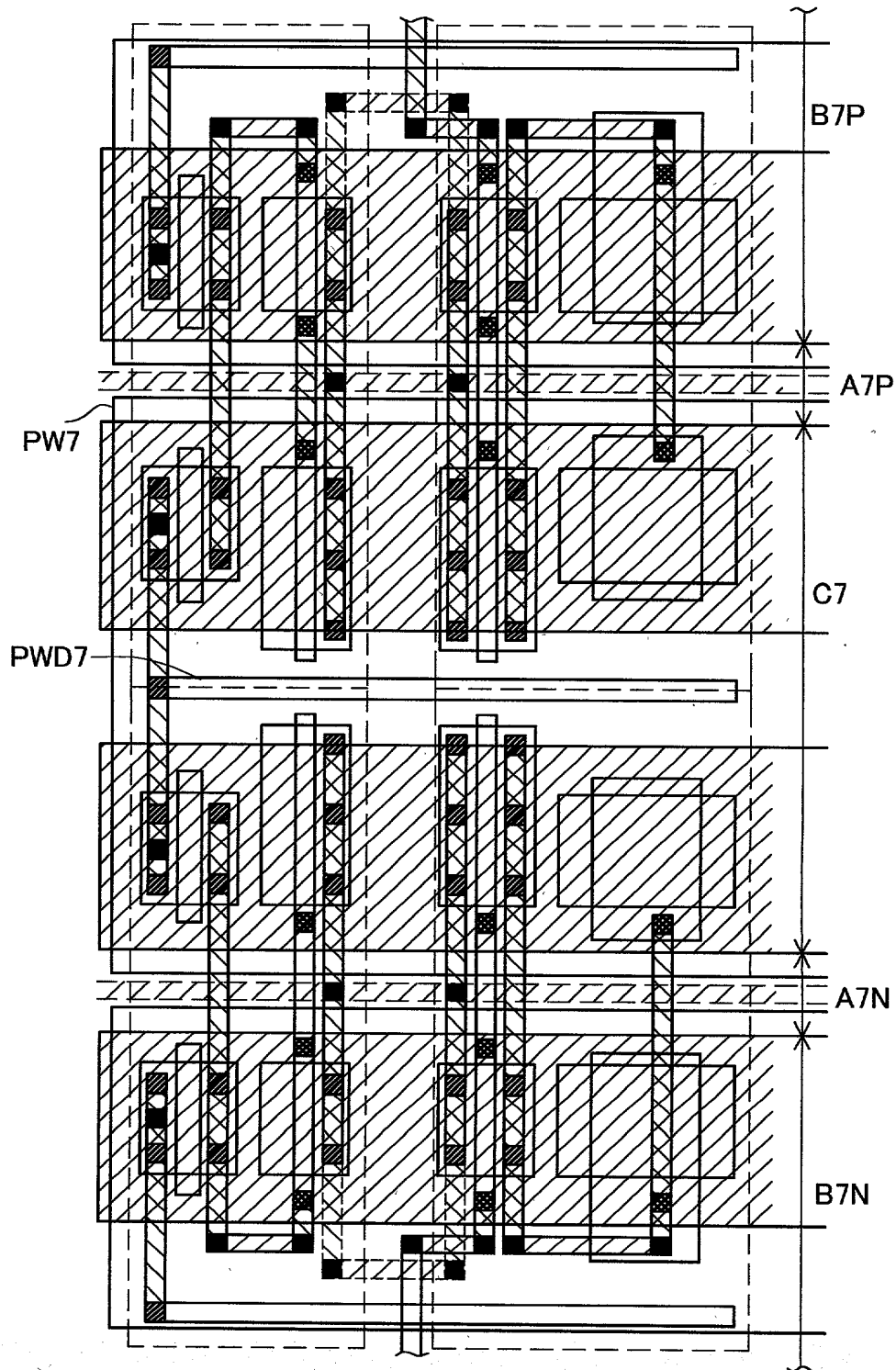


FIG. 8

FUNCTIONAL CIRCUIT DIRECTED TO FIG.23 LAID-OUT WITH MANNERS OF FIRST AND THIRD EMBODIMENTS

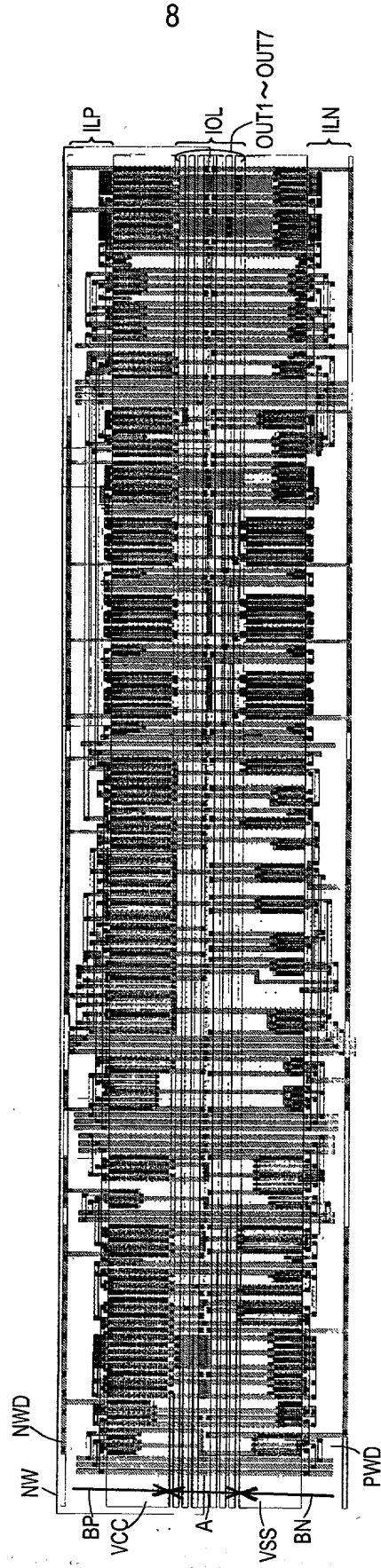


FIG.9 LOGIC CIRCUIT CIR1 DIRECTED TO FIRST AND THIRD EMBODIMENTS

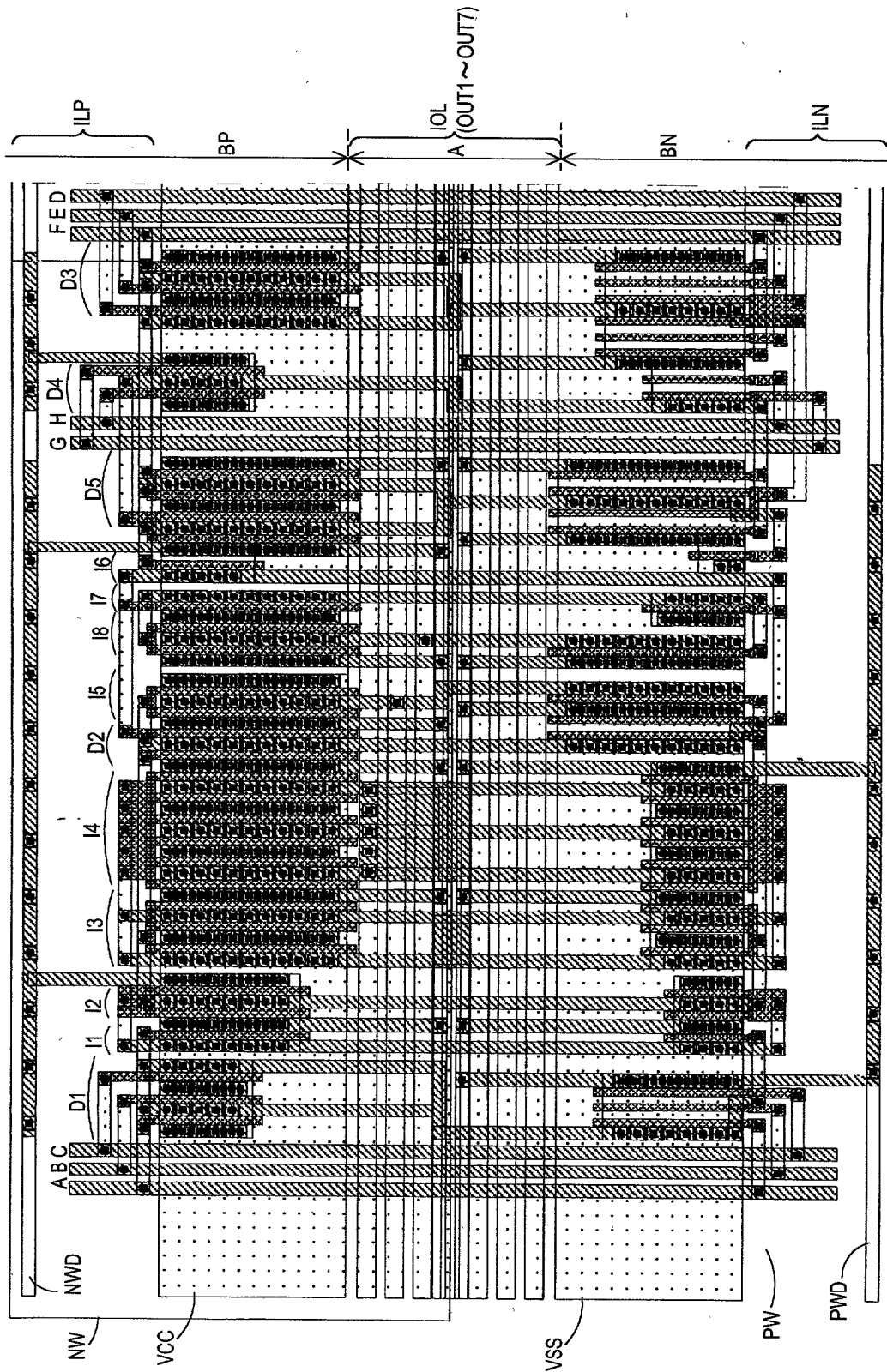


FIG. 10

LOGIC CIRCUIT CIR2 DIRECTED TO FIRST AND THIRD EMBODIMENTS

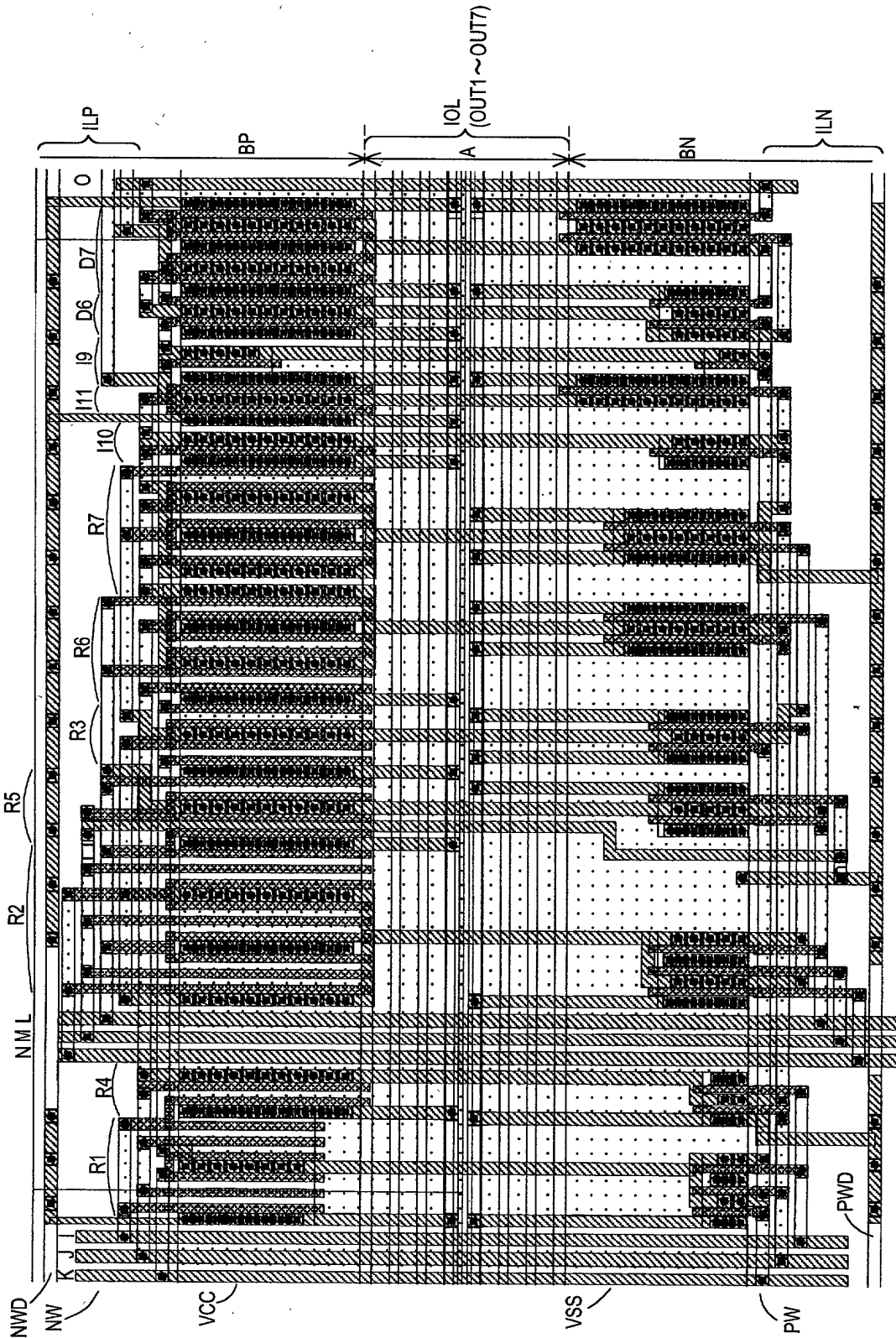


FIG.11

LOGIC CIRCUIT CIR3 DIRECTED TO FIRST AND THIRD EMBODIMENTS

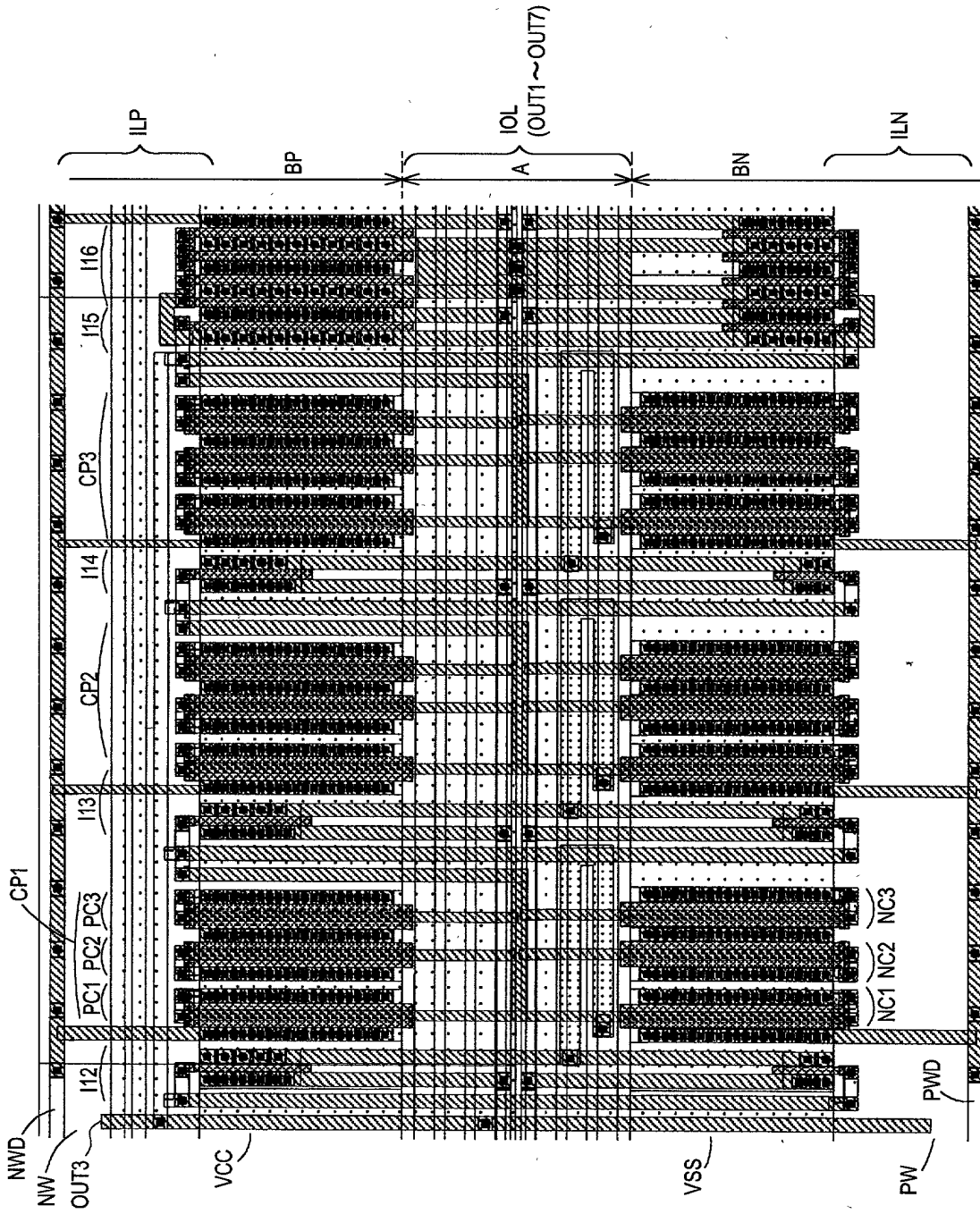


FIG. 12 LOGIC CIRCUIT CIR4 DIRECTED TO FIRST AND THIRD EMBODIMENTS

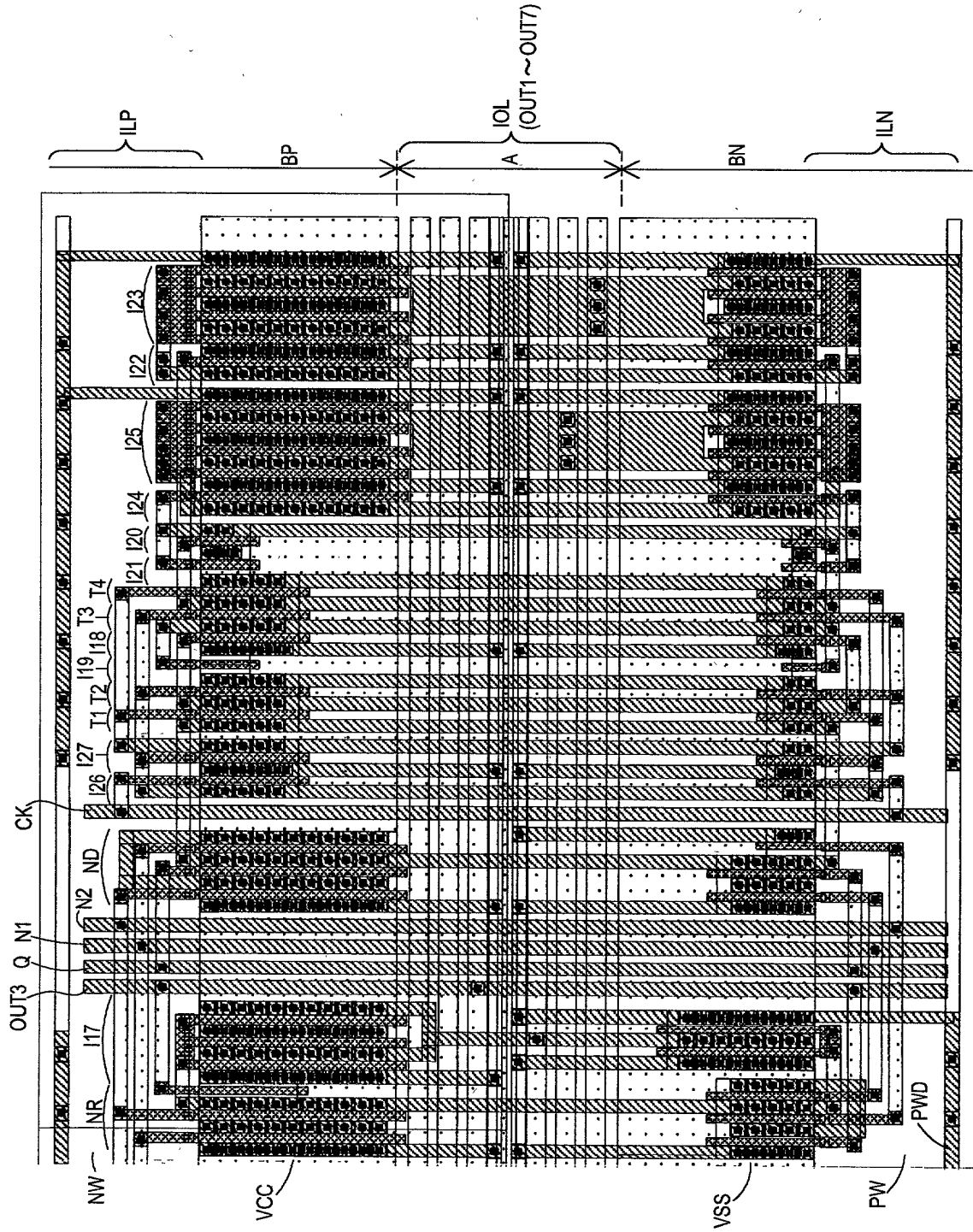


FIG.13

FUNCTIONAL CIRCUIT DIRECTED TO FIG.23 LAID-OUT WITH
MANNERS OF FOURTH EMBODIMENT

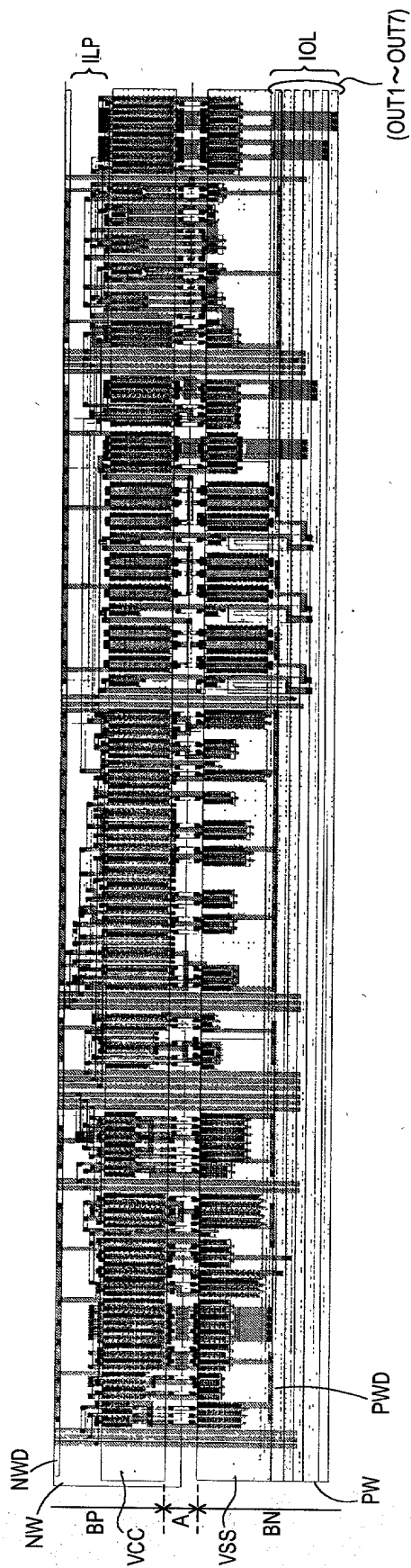


FIG.14

LOGIC CIRCUIT CIR1 DIRECTED TO FOURTH EMBODIMENT

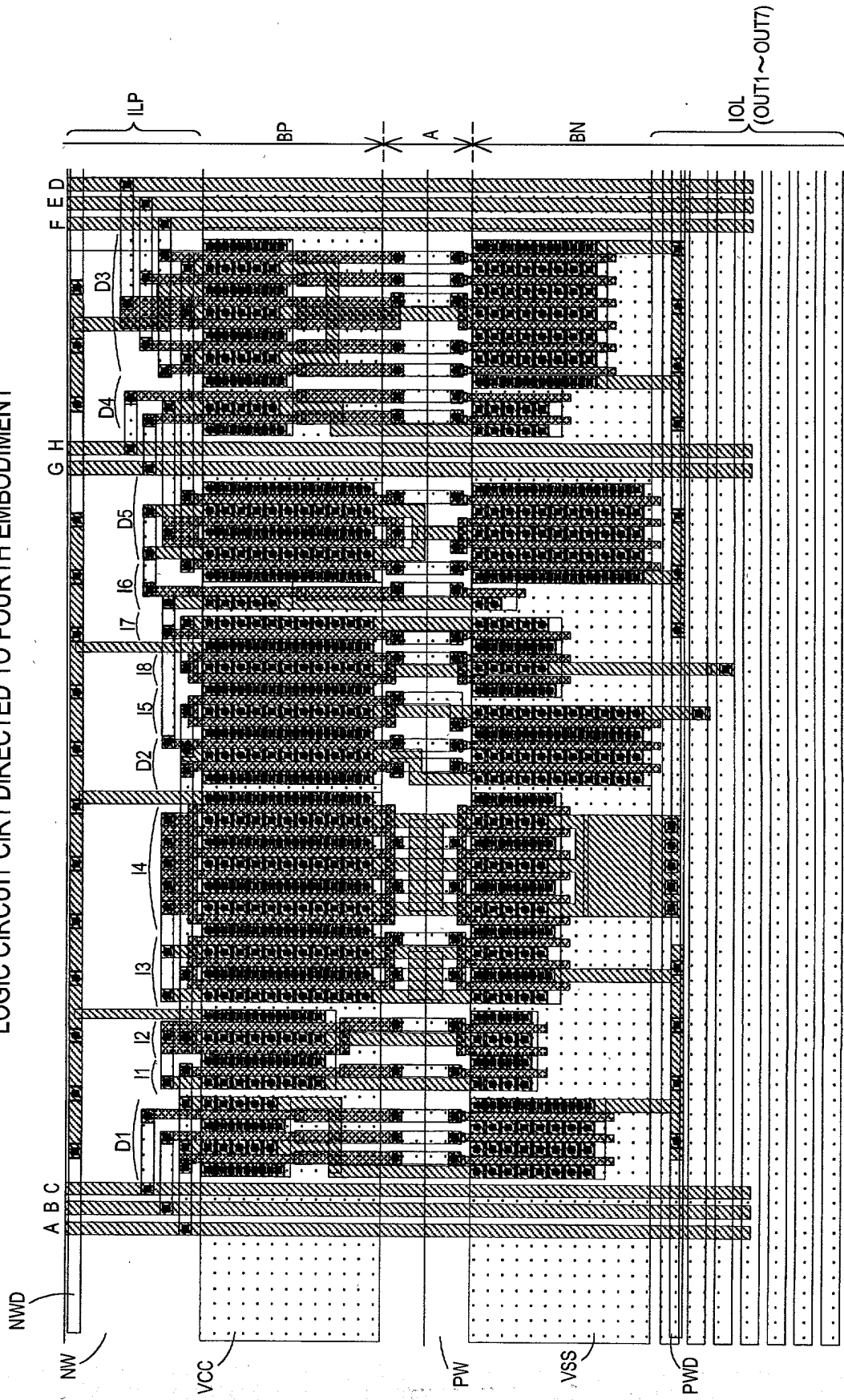


FIG.15

LOGIC CIRCUIT CIR2 DIRECTED TO FOURTH EMBODIMENT

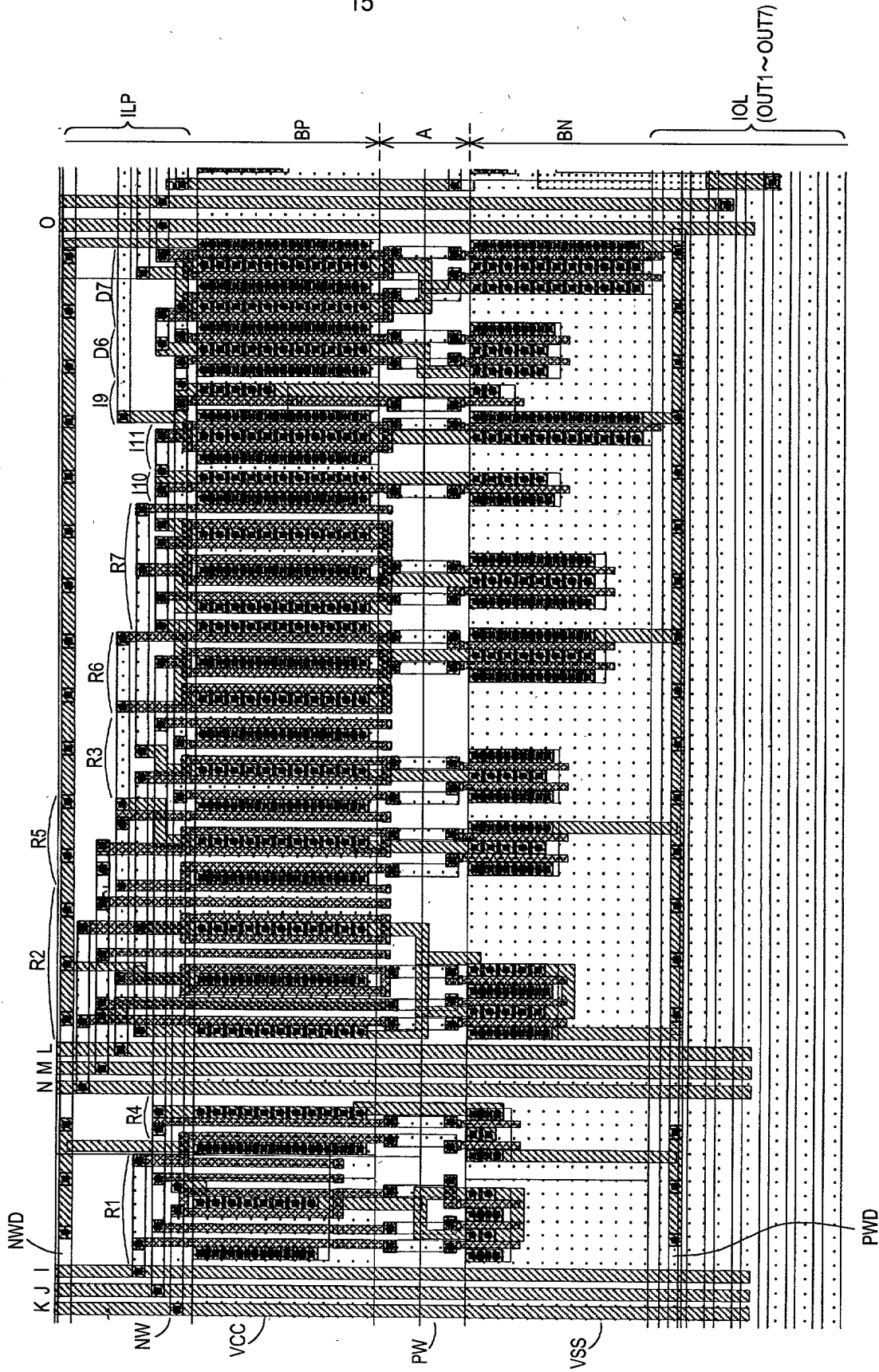


FIG. 16

LOGIC CIRCUIT CIR3 DIRECTED TO FOURTH EMBODIMENT

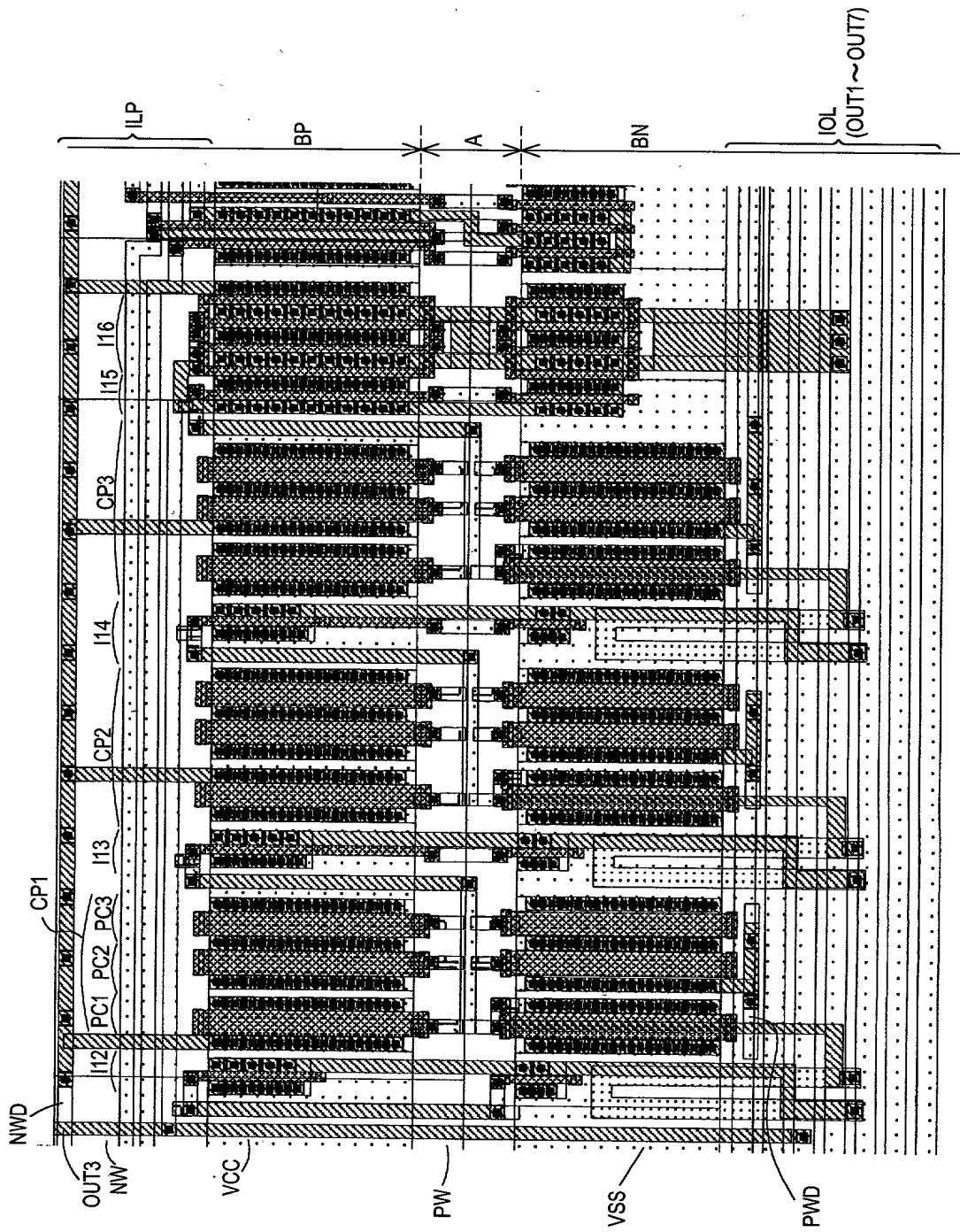
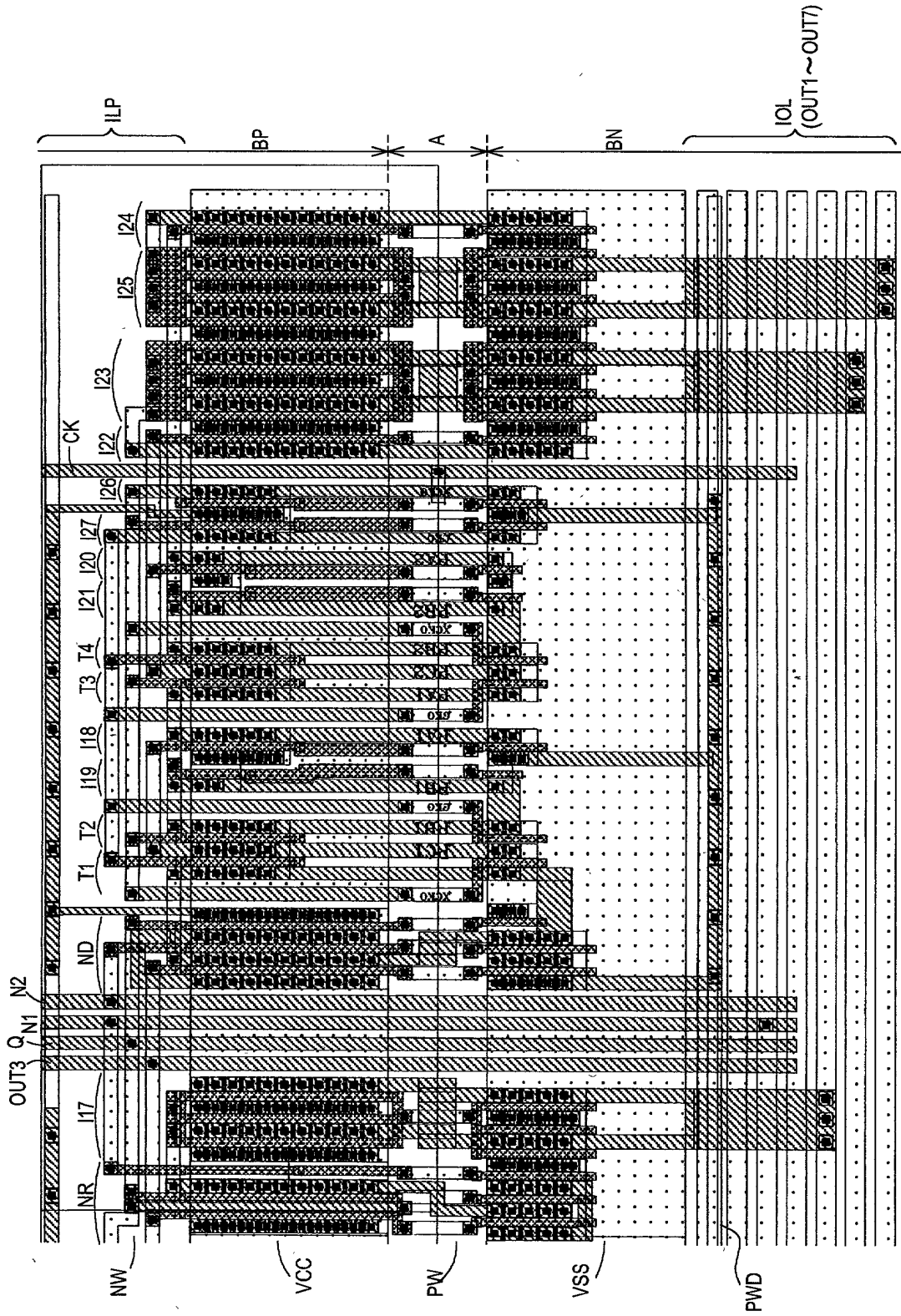
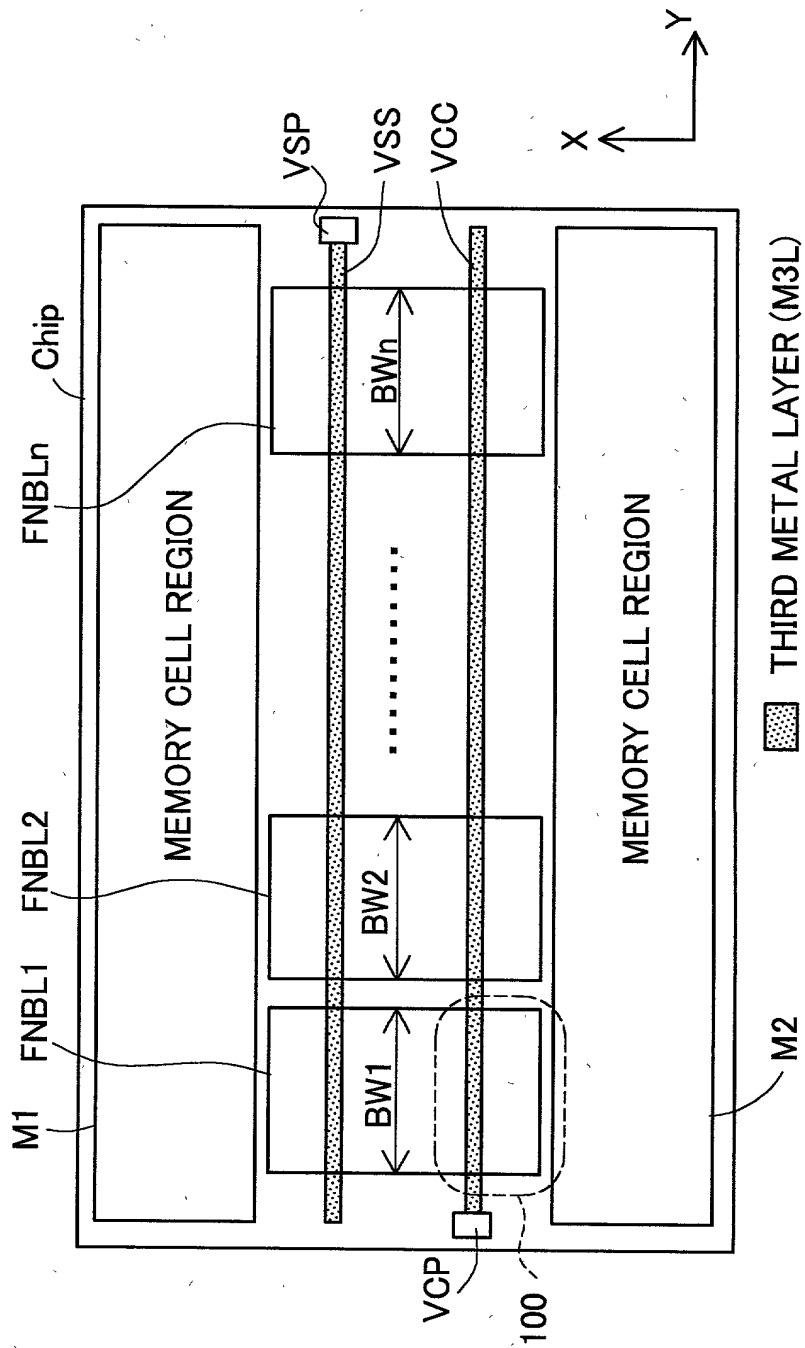


FIG.17

LOGIC CIRCUIT CIR4 DIRECTED TO FOURTH EMBODIMENT



LAYOUT OF FUNCTIONAL CIRCUIT GROUP ON SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



LAYOUT DIAGRAM SHOWING A PORTION FUNCTIONAL
CIRCUIT GROUP ENLARGED

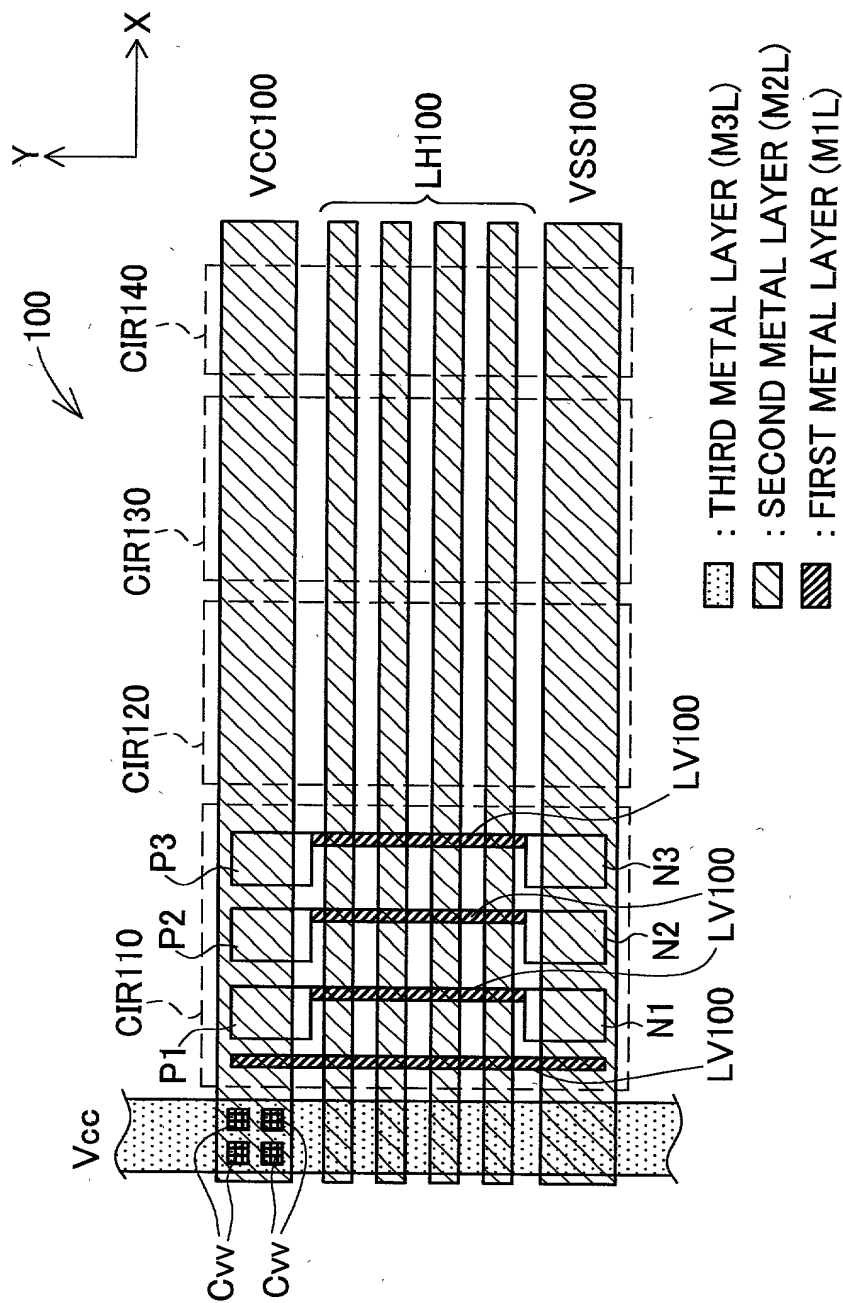


FIG.20

MULTI-LAYERED WIRING STRUCTURE AT EACH MANUFACTURING
PROCESS OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

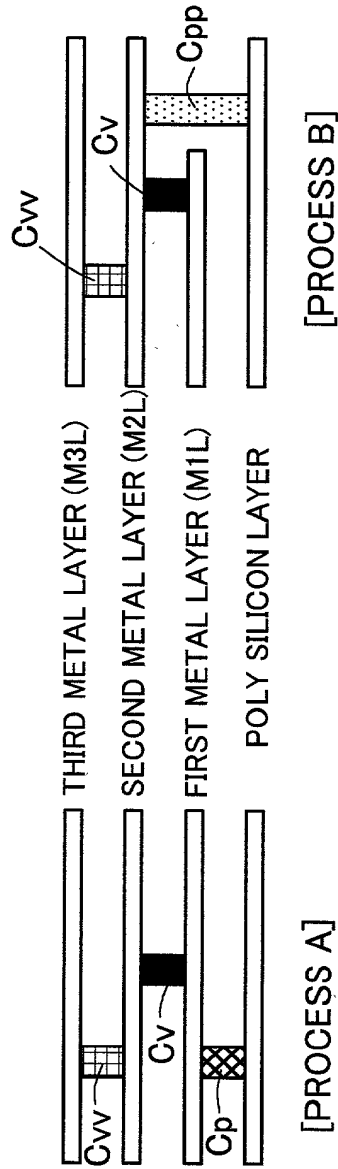


FIG.21 LAYOUT DIAGRAM IN CASE PROCESS A DIRECTED TO FIG.20 IS APPLIED

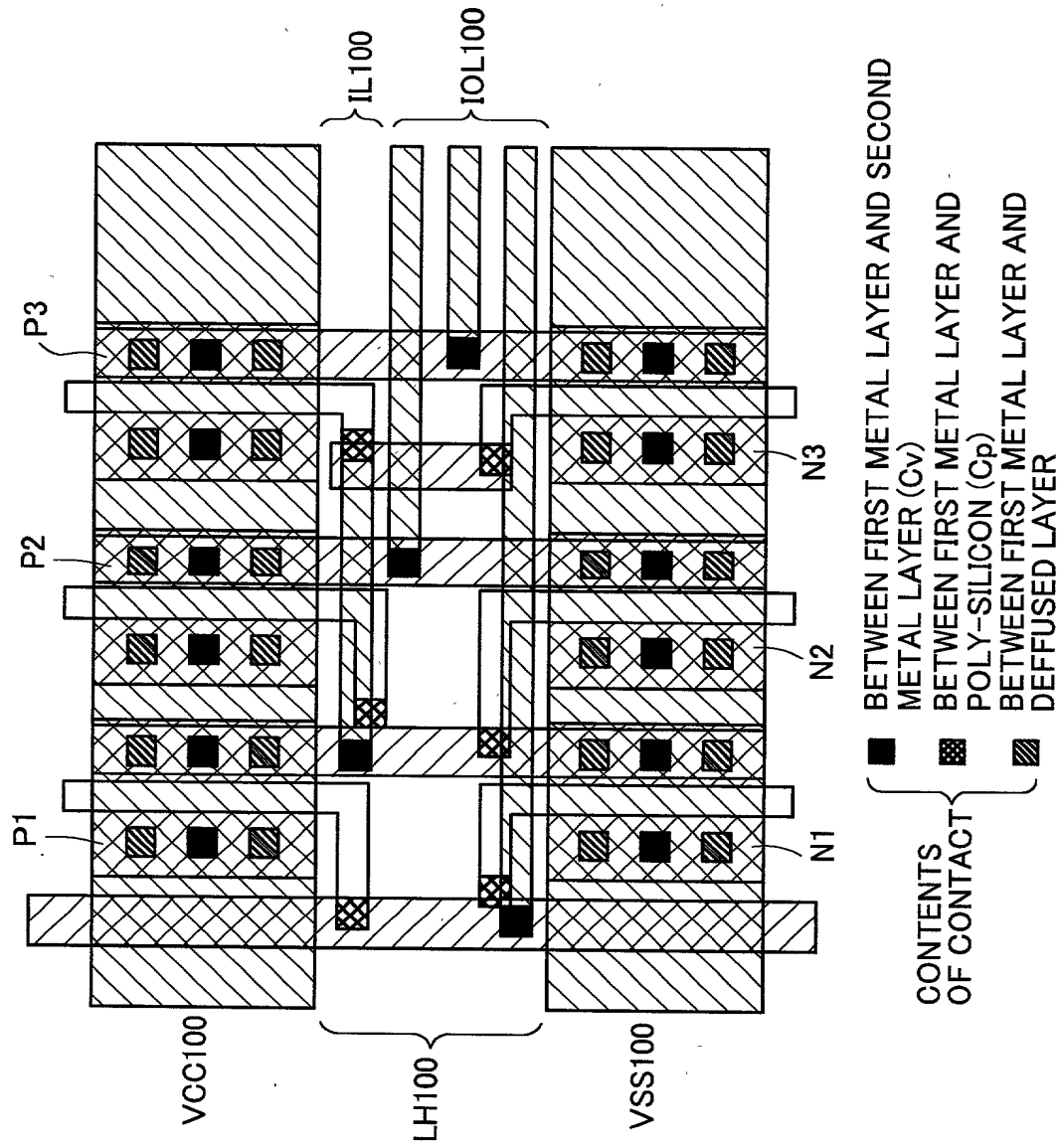


FIG.22

LAYOUT DIAGRAM IN CASE PROCESS B DIRECTED TO FIG.20 IS APPLIED

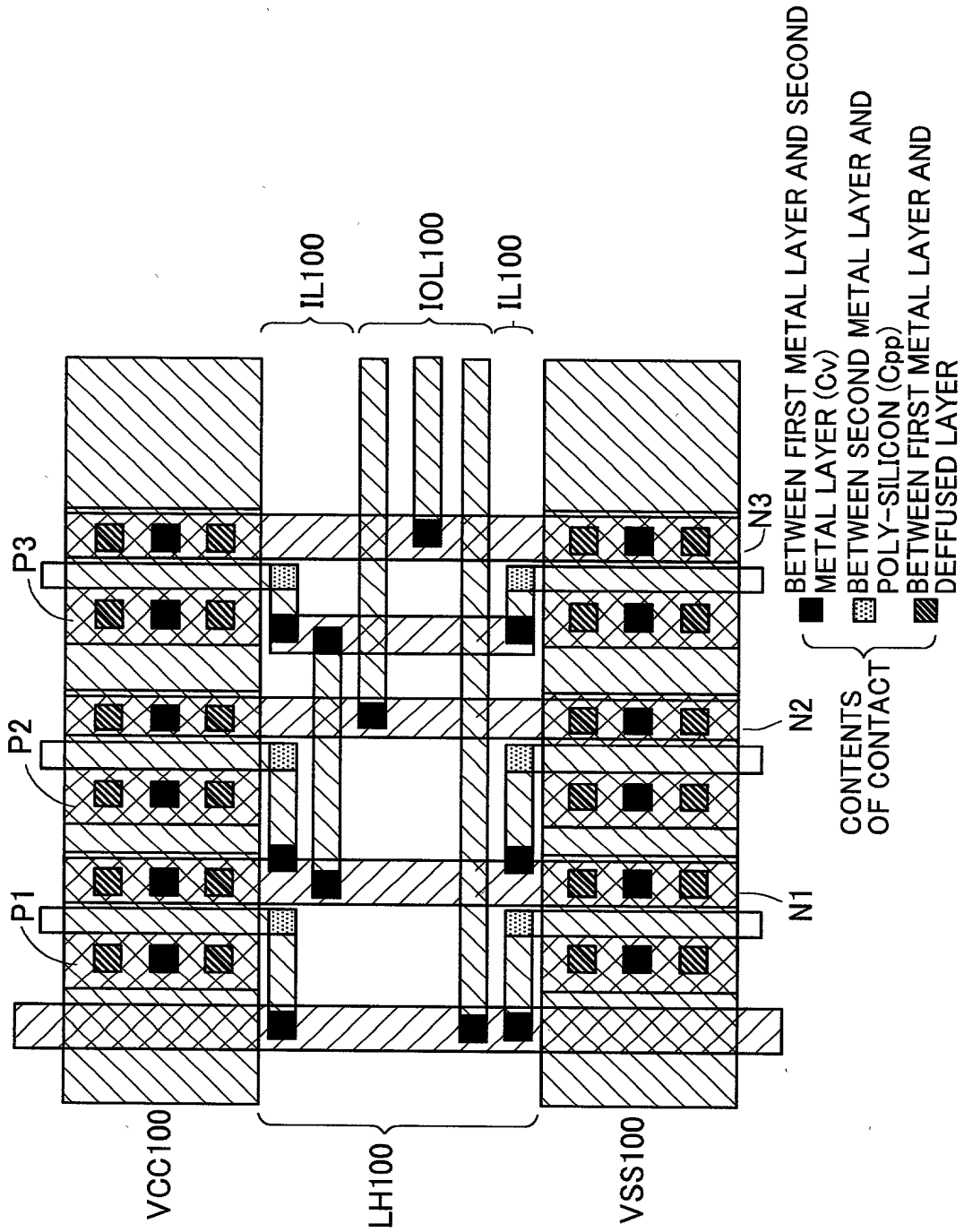


FIG.23

EXAMPLE OF FUNCTIONAL CIRCUIT

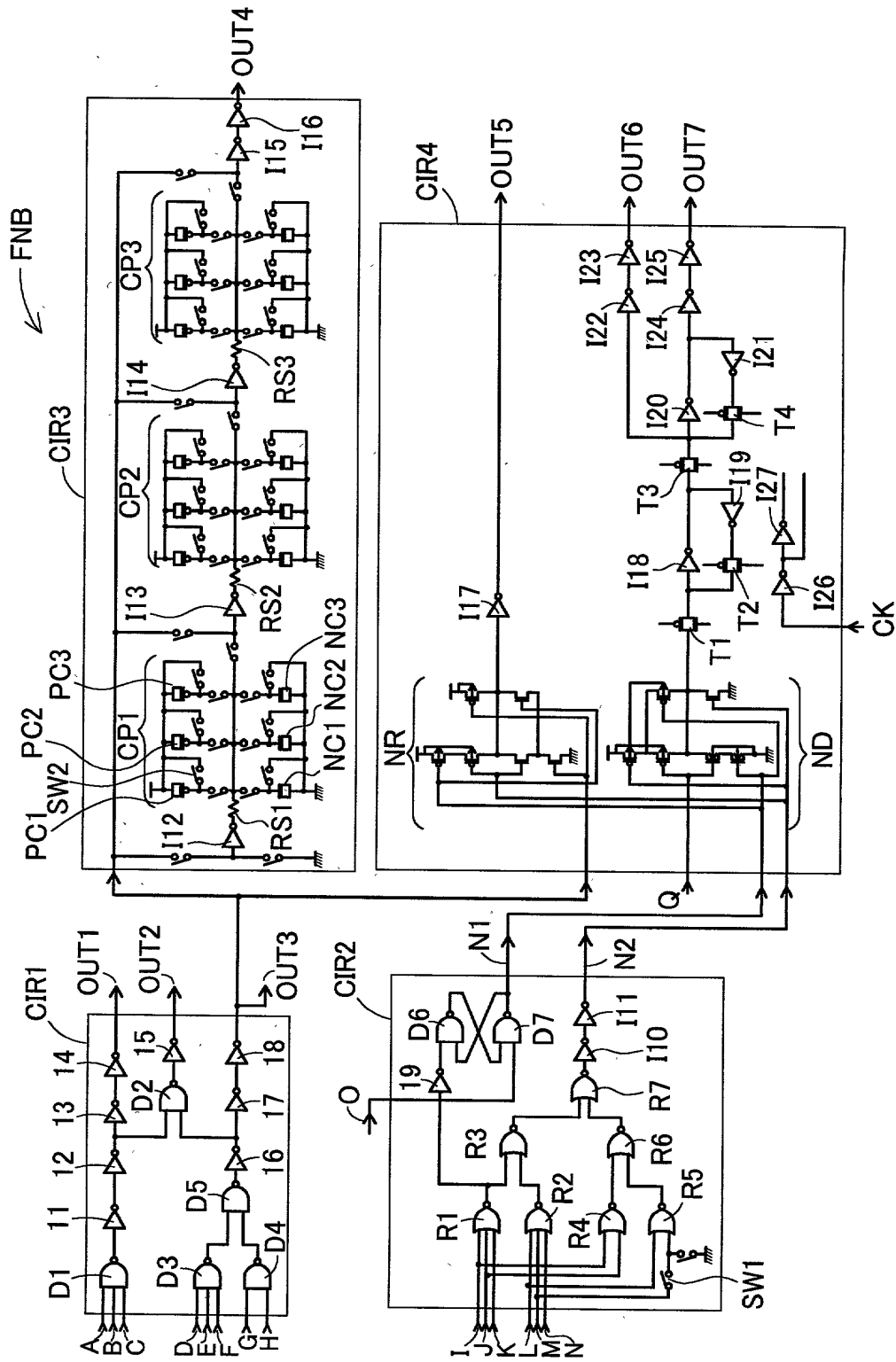


FIG.24 PRIOR ART

FUNCTIONAL CIRCUIT DIRECTED TO FIG.23 LAID-OUT WITH MANNERS OF PRIOR ART

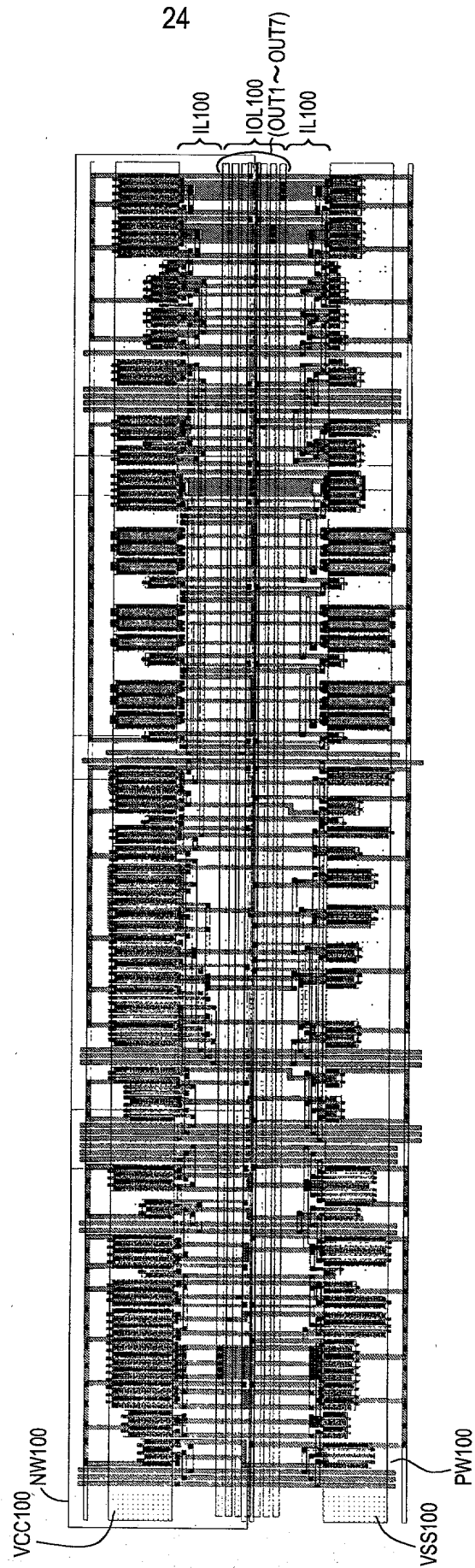


FIG.25 PRIOR ART

LOGIC CIRCUIT CIR1 DIRECTED TO PRIOR ART

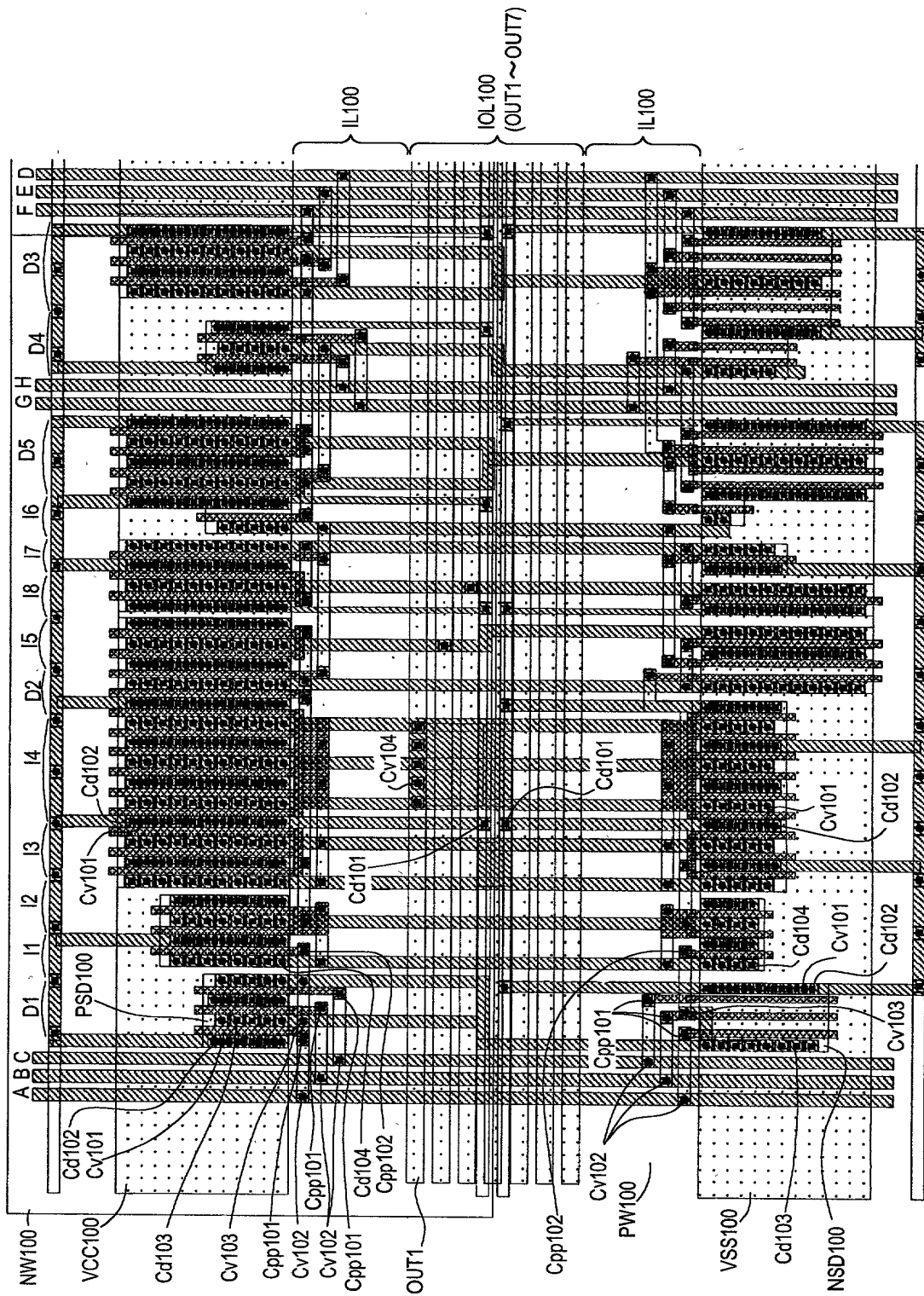


FIG.26 PRIOR ART
LOGIC CIRCUIT CIR2 DIRECTED TO PRIOR ART

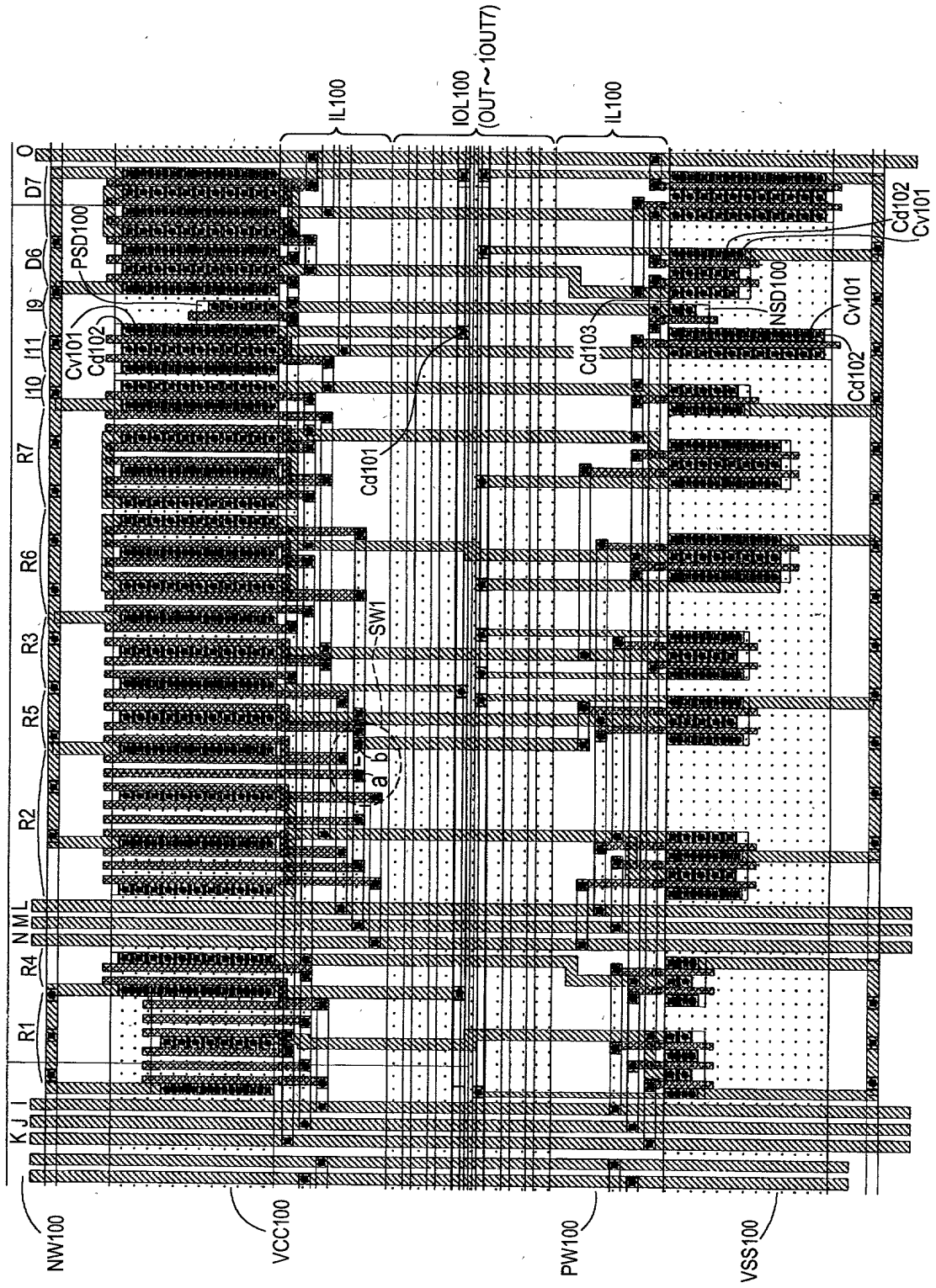


FIG.27 PRIOR ART

LOGIC CIRCUIT CIR3 DIRECTED TO PRIOR ART

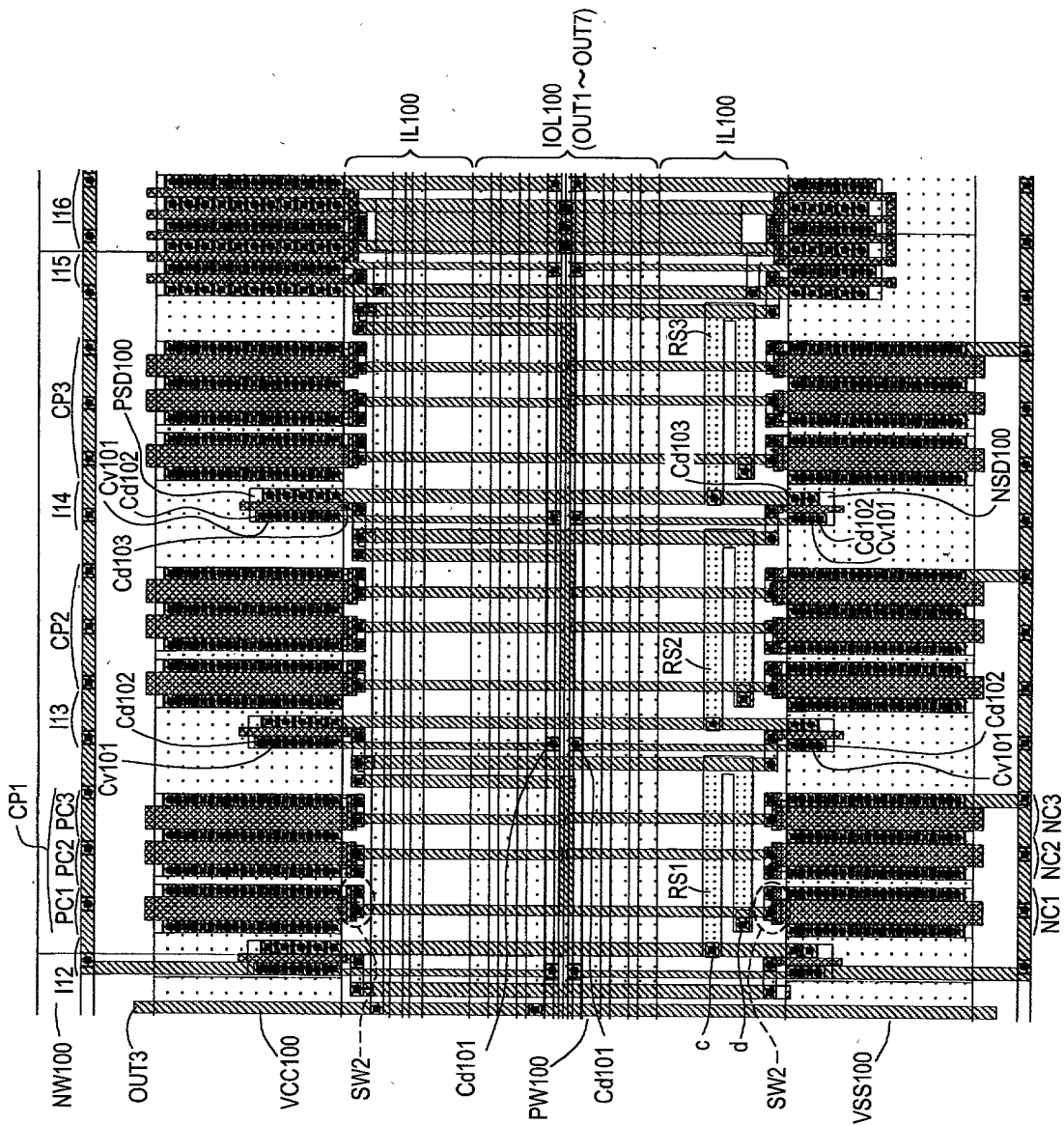


FIG.28 PRIOR ART

LOGIC CIRCUIT CIR4 DIRECTED TO PRIOR ART

